ICTS-String Theory Seminar

Title : Renormalized Circuit Complexity

Speaker : Aninda Sinha, Indian Institute of Science, Bangalore

Date : Thursday, July 25, 2019

Time : 11:00 AM

Venue : Emmy Noether Seminar Room, ICTS Campus, Bangalore

Abstract : We propose a modification to Nielsen's circuit complexity, where the minimum number of gates to synthesize a desired unitary operator is related to a geodesic length in circuit space. Our proposal uses the Suzuki-Trotter iteration scheme, usually used to reduce computational time cost, which provides a network like structure for the circuit. This leads to an optimized gate counting linear in the geodesic distance unlike in the original proposal. We show how a renormalization beta-function type equation can be written for the penalty factors where the role of the RG scale is played by the network depth, which itself is correlated with the tolerance. The density of gates is shown to be monotonic with the tolerance and a holographic interpretation arising from c-theorems is given. This picture appears to be closely connected with the AdS/CFT correspondence via path integral optimization.